Amendments to the Claims

1. (Original) A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

forming said transistor structure so as to be conductively coupled to said word line;

forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug so as to define a substantially convex upper plug surface profile in contact with said bit line.

2. (Original) A method of manufacturing a memory cell as claimed in claim 1 wherein said insulating side walls are formed so as to comprise a first pair of opposing insulating side walls along said first dimension and a second pair of opposing insulating side walls along said second dimension.

3. (Original) A method of manufacturing a memory cell as claimed in claim 2 wherein said first pair of opposing insulating side walls are formed so as to comprise respective layers of insulating spacer material formed over a conductive line.

4. (Original) A method of manufacturing a memory cell as claimed in claim 2 wherein said second pair of opposing insulating side walls are formed so as to comprise respective layers of insulating material formed between respective contact holes.

5. (Original) A method of manufacturing a memory cell as claimed in claim 1 wherein said contact hole is filled with said polysilicon plug to an uppermost extent of said insulating side walls.

6-9. (Canceled)

10. (Withdrawn-Currently Amended) A method of manufacturing a memory cell as claimed in claim 1, wherein ~~comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:~~

~~forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;~~

~~forming said transistor structure so as to be conductively coupled to said word line;~~

~~forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and~~

~~forming~~ said doped polysilicon plug is formed by partially filling said contact hole with said conductively doped silicon plug such that said plug defines a substantially convex upper plug surface profile in contact with said bit line.

11-13. (Canceled)

14. (Withdrawn-Currently Amended) A method of manufacturing a memory cell as claimed in claim 1, wherein said method further comprises ~~comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising~~ the steps of:

~~forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;~~

~~forming said transistor structure so as to be conductively coupled to said word line;~~

~~forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls;~~

~~forming said doped polysilicon plug so as to define a substantially convex upper plug surface profile in contact with said bit line;~~

forming a storage node such that it is characterized by a storage node contact hole bounded by insulating side walls; and

filling said storage node contact hole with a conductively doped polysilicon plug such that said storage node plug defines a substantially convex upper plug surface profile.

15-18. (Canceled)